1. Single Crystal, CVD Diamond and fast timing*

2. Fast Electronics for TOF and Energy Spectroscopy:
extracts from NoRHDia Workshop 31 Aug-1 Sept 05

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* Some images have been removed from this summary, as the work is subject to a Non-Disclosure Agreement with an industrial partner. For further information, contact morse@esrf.fr

why diamond?

Z = 6, à low specific X-ray absorption/beam scattering

High charge-carrier saturation velocity (~3×10^7 cm/s),
low dielectric constant (5.5)

à fast pulse response (~nsec in practical devices)

wide bandgap energy (5eV), excellent thermal/mechanical properties

à high heat load, 'pink' beam monitoring possibilities

why single crystal material ?

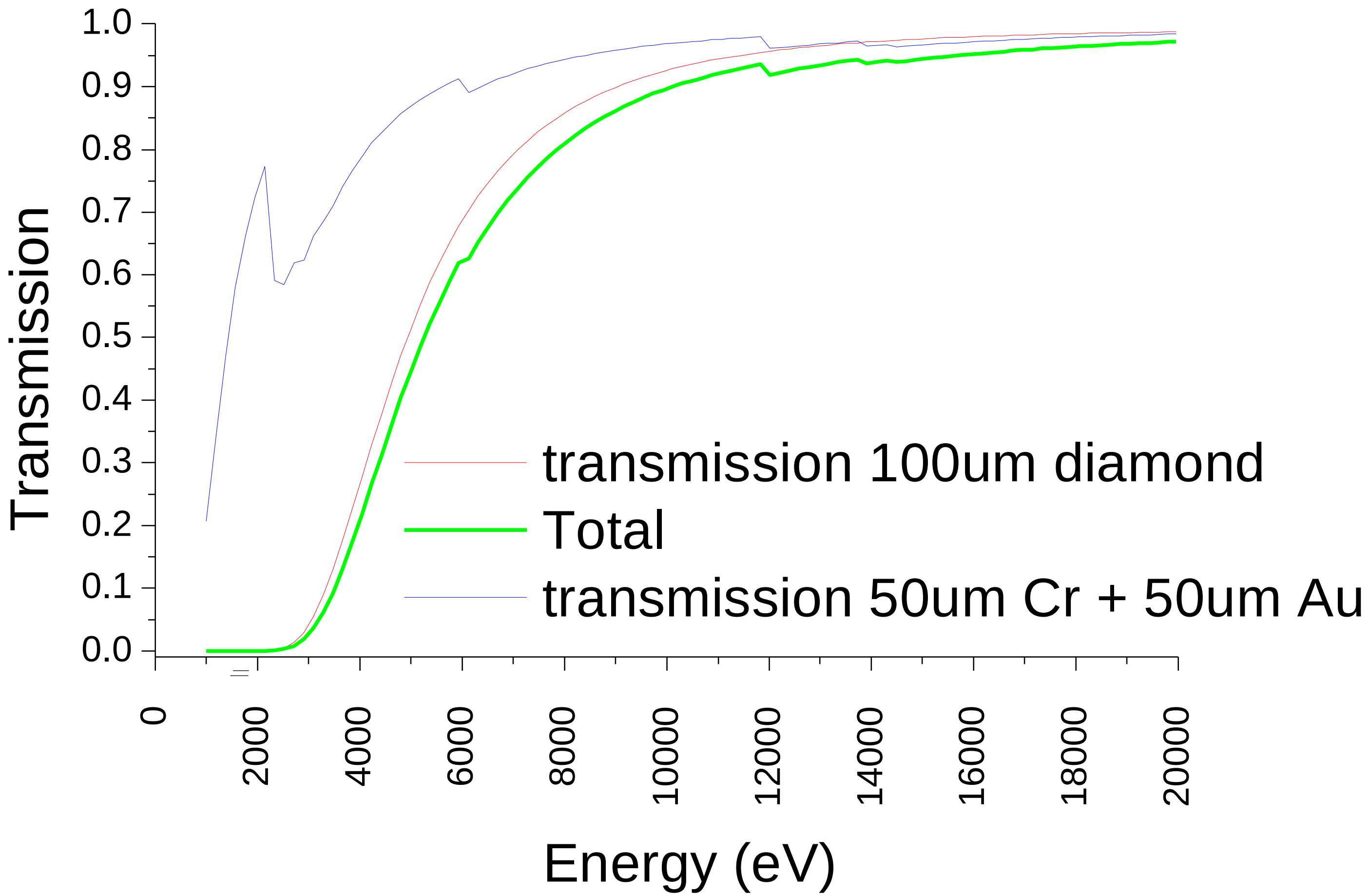
uniform response (cf. grain-boundary artifacts and trapping in polycrystalline CVD diamond

charge-carrier lifetime >50nsec

(à 100% charge signal collection over > mm distances)

Material absorption limitations

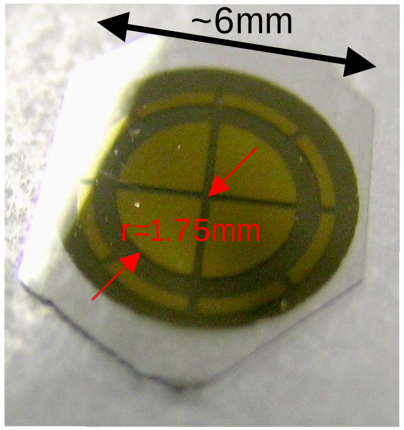
Diamond with metal contacts

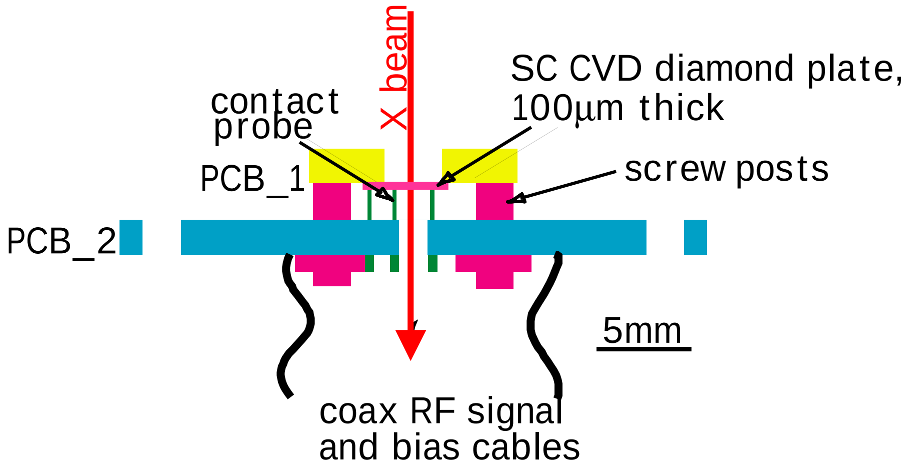


Quadrant design test at ESRF-ID21 (May 2005)

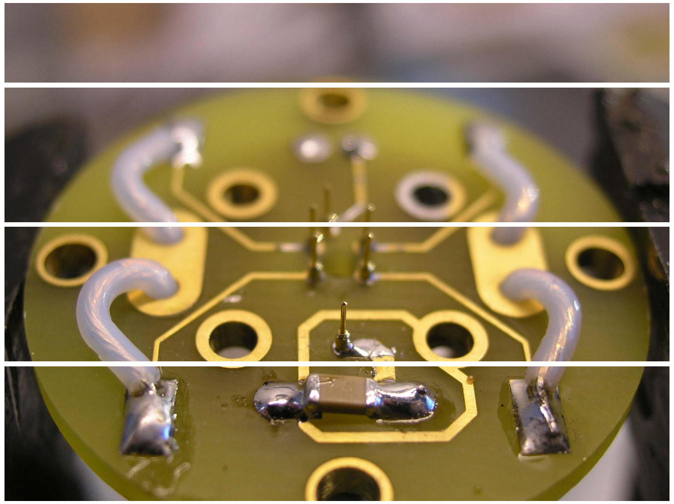
Plate thickness
100micron [E6]

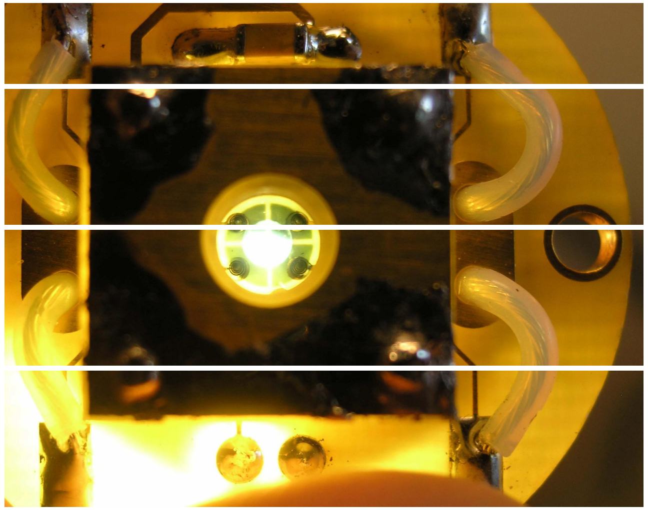
20nm+20nm
Cr, Au contacts
[GSI-Darmstadt]





PCB assemby
with sprung
microprobes ,
'RF compatible'
layout





Spatial Uniformity

Individual ‘dc’ quadrant signal currents as microbeam raster-mapped over surface

‘composite’ response

beam 1 x $0.4\mu^2$ fwhm, ~10^8 photos/sec at 7keV

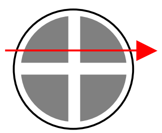
-BPM

For small beam size (< 20µm), signal slope is convolution of charge collection diffusion, photoelectron range…).

‘C of G’ sensitivity <0.1µm

For large beam (> 20µm), response is defined ‘geometrically’ simply as ‘beam crossing a thin line’

signal slope ~5% (80pA) /micron



Line scans, ~10^8 photons/sec @7keV

signal slope ~0.5% (250pA) /micron

line scan, ~$3x10^9$ photons/sec @7keV

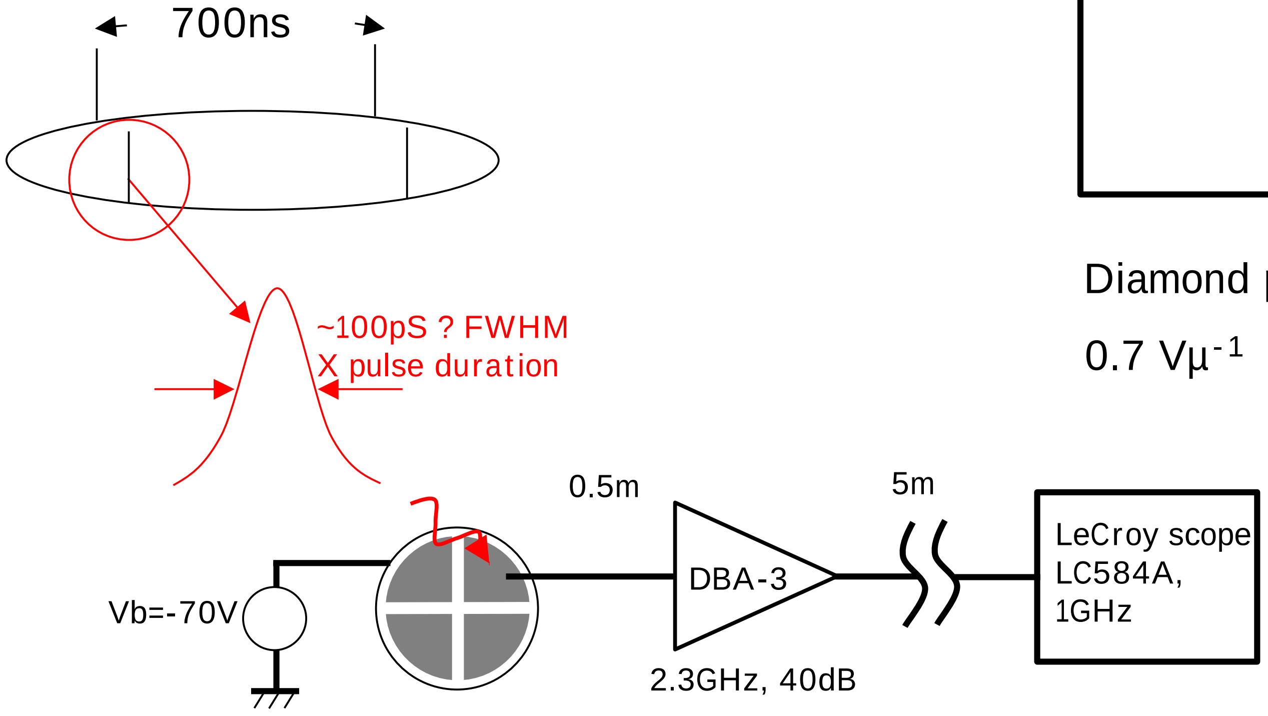
Signal linearity with X ray beam intensity

Linear over > 3 orders (this experiment)

Maximum 'diffusion' current density' measured ~1 mA/cm^2 dc equivalent (>0.1 A/cm^2 peak for ~2ns charge collection pulse width)

Time response: signal from an individual X-ray bunch

ESRF synchrotron in
4 bunch mode



Diamond plate 100µm thick,

0.7 $V\mu^{-1}$

Individual signal pulses correspond to ~160 X-rays @7.2keV absorbed in diamond plate, i.e. total signal pulse energy ~1MeV (~15fC)

Signal pulse shape:
bias and beam position

200µmØ beam centered on the upper left electrode:

Pulse shape full width is 'consistent' with 60(45)µm/ns @ 0.5V/µm hole(electron) drift velocities*

not saturated drift velocity!

'Split signal' (beam centered in quadrant isolation gap:

signal shape ~same, with amplitude (measured on one quadrant) simply halved.

*Pernegger et al, J. Appl. Phys. 97, 073704 (2005)

Is there a role for diamond as a ‘T_o’ detector ??

- using transimpedance preamp, timing precision determined by preamp risetime and energy signal/noise

should be <<100psec for detector area
~ few mm^2 (capacity ~1 pF for 100µm thickness)

- For diamond plate in beam as Io monitor, energy signal/noise may approach beam sample statistics limit…

à pulse-by-pulse I_o normalization of data ?

Fast Electronics for TOF and E-Spectrometry
- some recent NoRHDia presentations
(relevant to Synchrotron NRS ??)

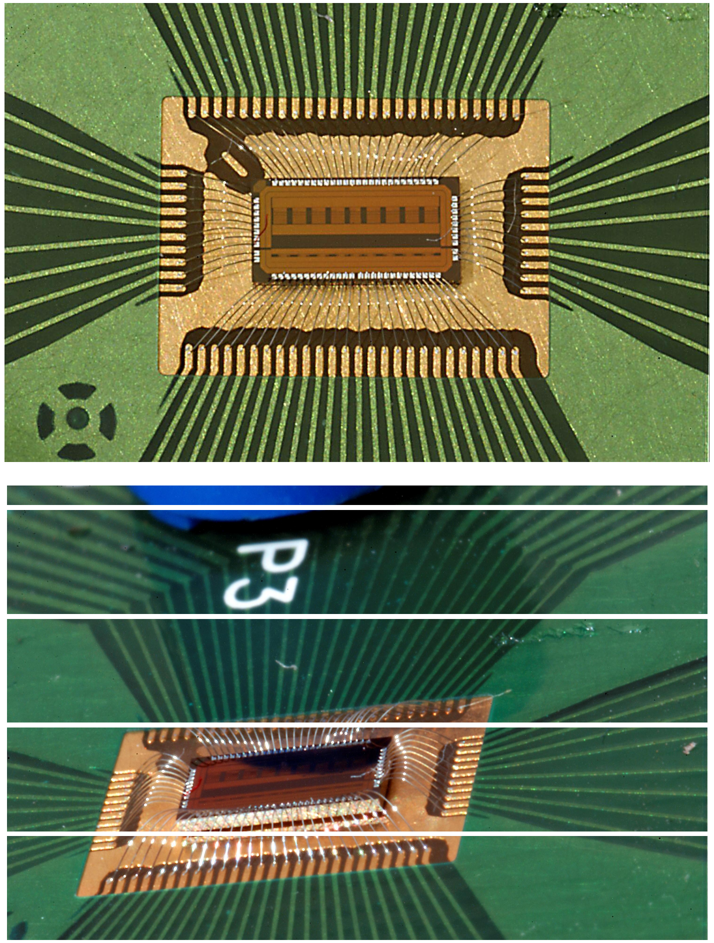
1. NINO: 'an ultra-fast, low-power, preamplifier-discriminator'

2. Time Stamping: an ASIC design for a ring-oscillator TDC

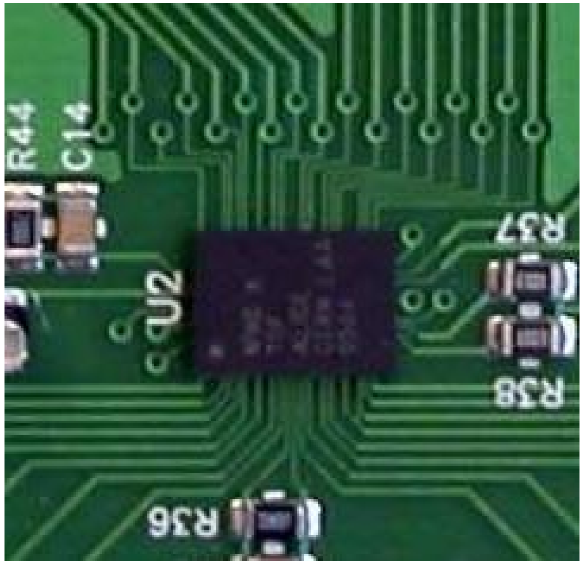
NINO, an ultra-fast, low-power, front-end amplifier discriminator

courtesy E. Usenko, INR RAS, Troitsk, Russia

- IBM 0.25 um Si CMOS technology
- 8 channels, 2x4 mm^2 chip
- Channel power is 27mW
- +2.5V supply voltage only
- Delay time 1ns
- Easy operating and controlling



The NINO ASIC bonded to PCB



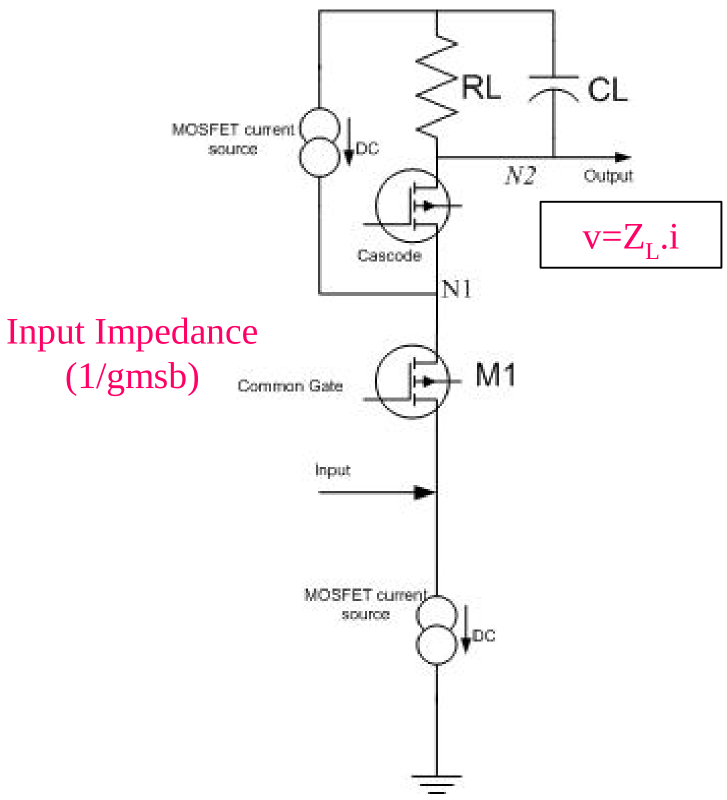
The NINOTAPP final package

produced for Cern ALICE detector RPC readout, 160k channels

- Common gate circuit with very high bandwidth @<0.5ns peaking time

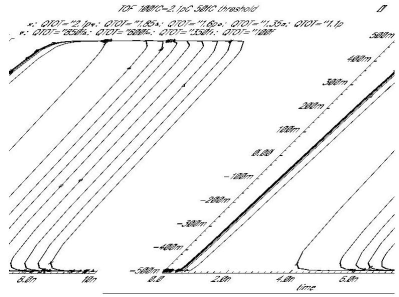
- Input impedance (1/gmsb) is tuned to match the impedance of detector signal transmission lines

- No signal feedback, fully differential DC coupled structure is ideal for high data rates and large signals dynamic range.

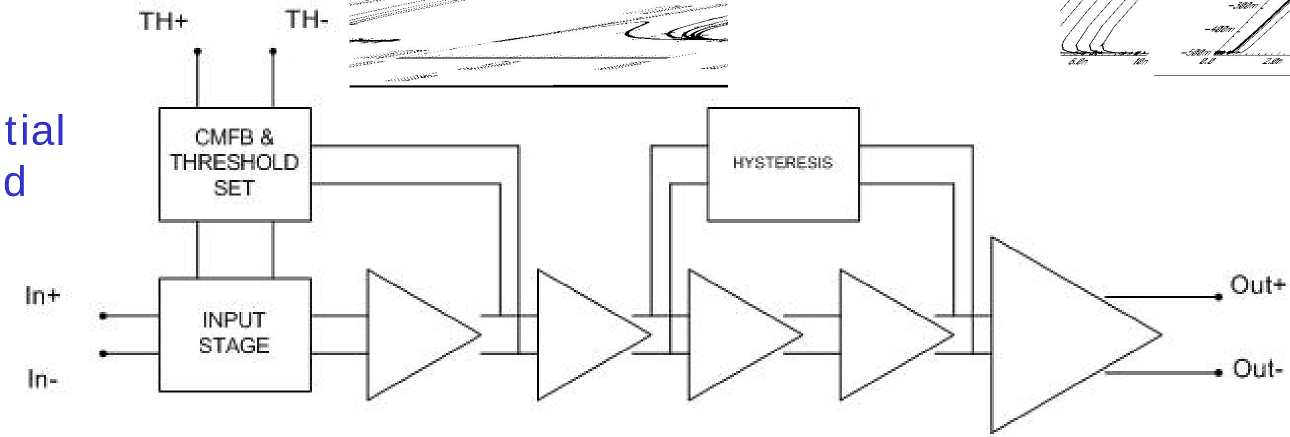


Input stage (half of fully differential circuit)

NINO channel structure



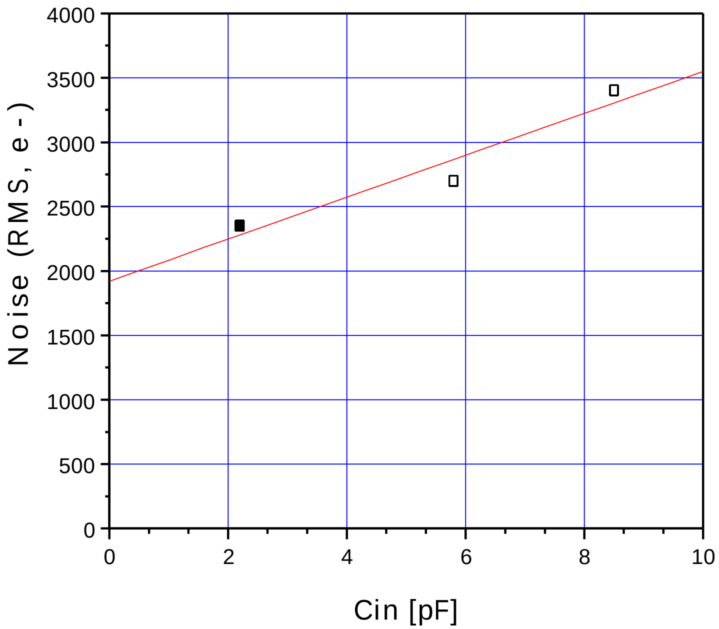
Differential front end input



LVDS outputs

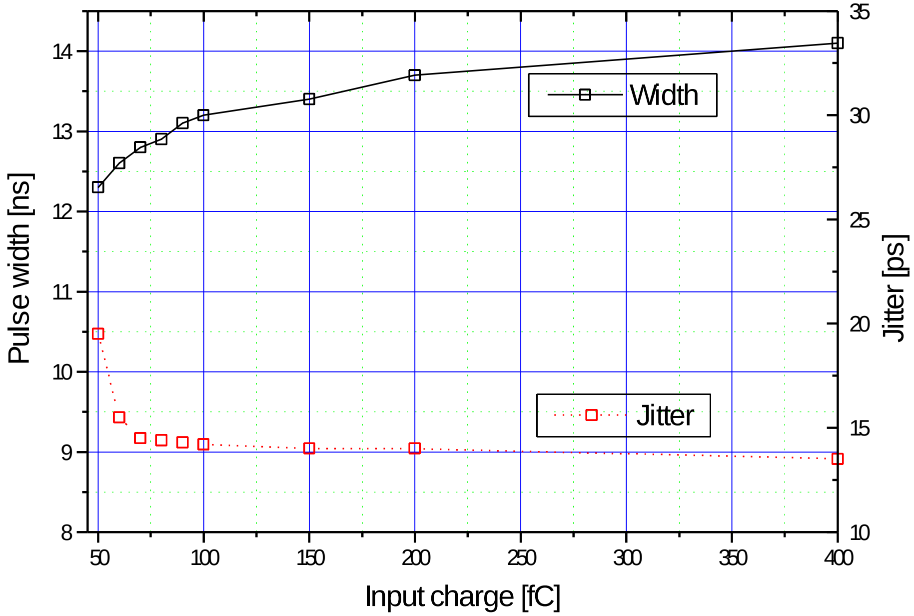
- Minimum threshold at 5-10fC.
- < 3000 el. Noise @ 6pF Cdet
- Tunable differential input impedance on the range (40-100) Ohm.
- < 9 ps rms front edge time jitter
- Hysteresis value can adjust up to 12%
- Pulse width variable from 0.5ns up to 6ns vs. input charge.

Noise vs. Cin for liner range



Jitter & Pulse width vs. charge (LeCroy pulser)

Setup: Uth=120 mV, Uhys=0 V, Ustr=1,2 V, Rext=25 Ohm

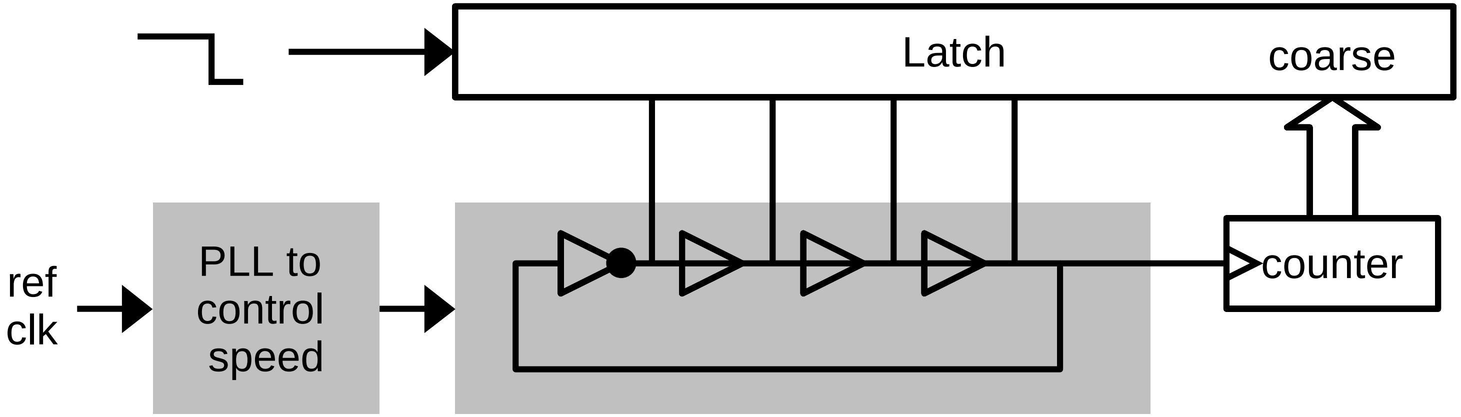


- < 3000 el. Noise @ 6pF Cdet,
- Rext is 25 Ohm
- Input DC offset voltage (equivalent of amplification factor) limits minimum detectable charge to 5-10 fC

- equivalent input charge is 30fC,
- Rext is 25 Ohm,
- additional stretch time value is 12ns

Time Stamping: a Ring Oscillator TDC

Courtesy Peter Fischer, Michael Ritzert, Inst. für Techn. Informatik,Univ. Mannheim

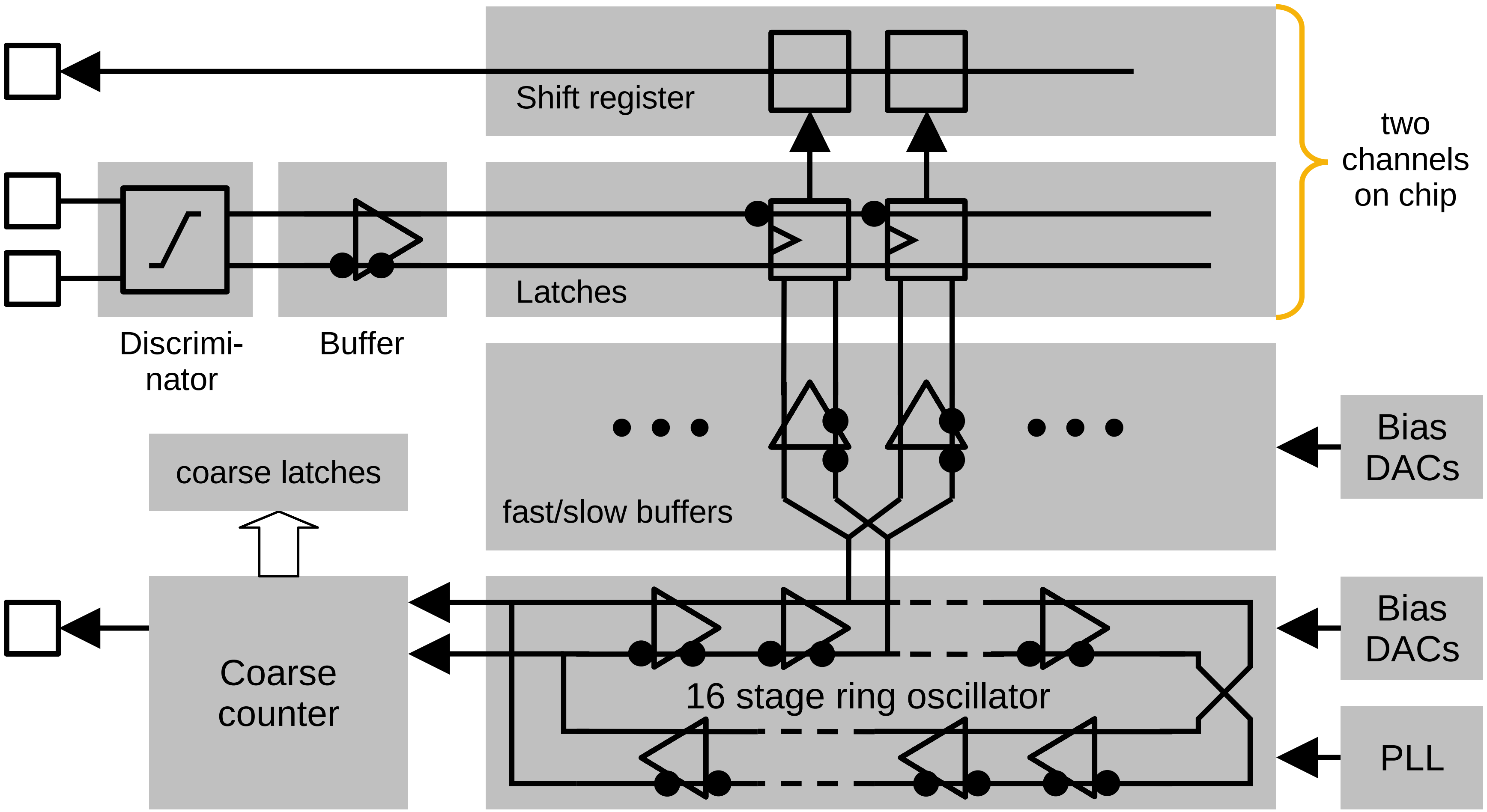


- a ring oscillator generates thermometer code time stamps. Needs overall inversion!
- a ('slow') coarse counter generates the MSBs
- input signal is used to latch values
- Ring oscillator can be locked to a reference clock with a PLL

+ fairly simple, 'digital' design
+ infinite dynamic range
+ no calibration required (with PLL), guaranteed stability
- limited bin size (but several times better than with counter)

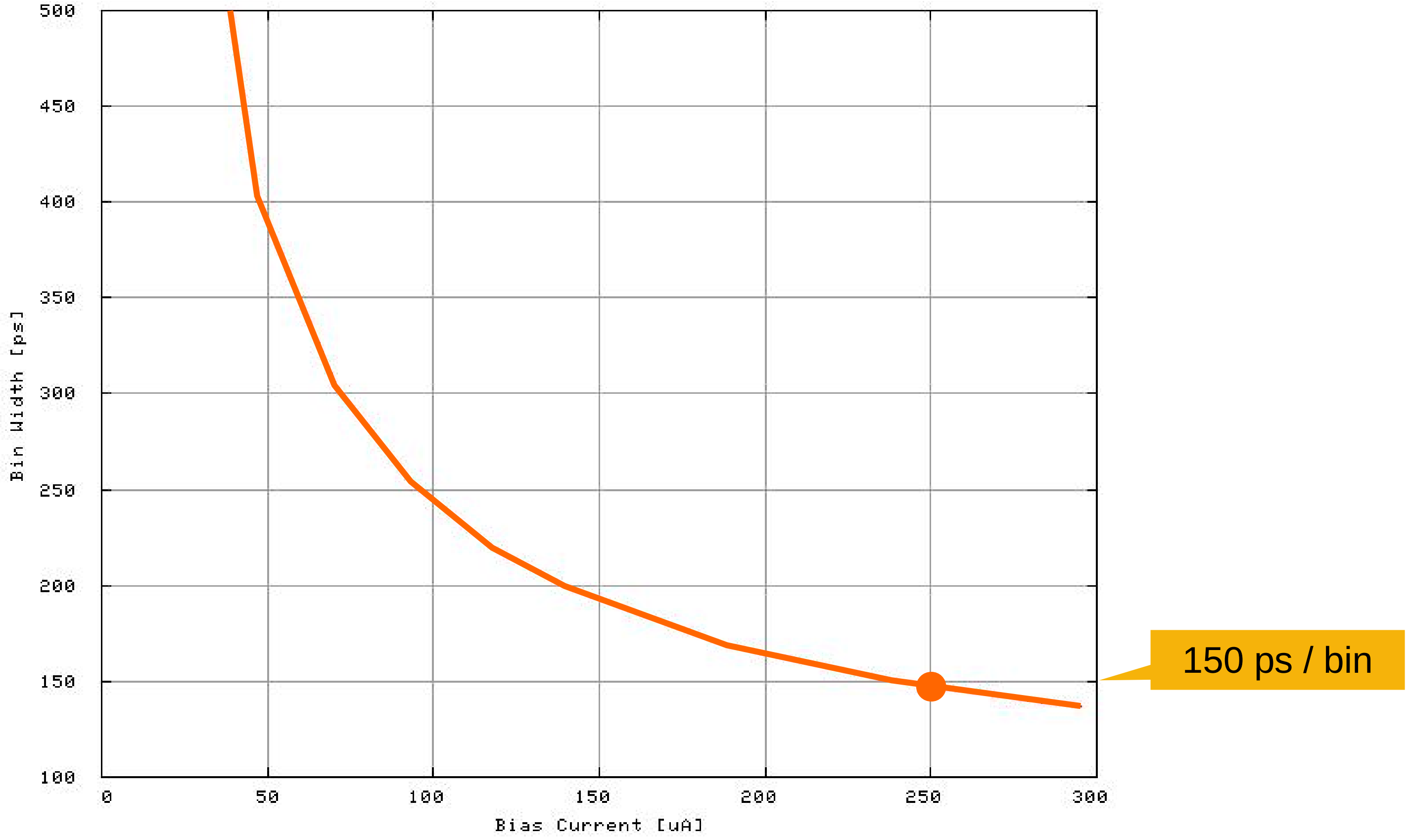
AMS 0.35µm Test Chip ‘TC3’

- Block diagram shows only relevant parts
- differential inputs have an additional (analog) discriminator



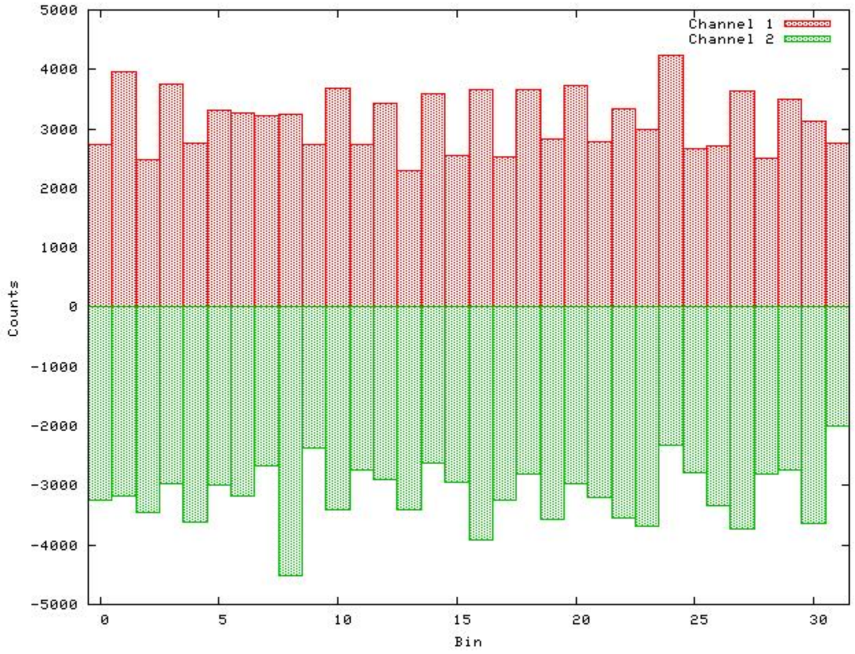
Measurements: Ring Oscillator Speed

- 16 stage Ring oscillator speed can be measured on a scaled down digital output
- Speed can be tuned in a wide range as a function of bias current (per stage)
- Standard operation point: **150 ps / bin**



Bin occupancies (i.e. relative bin width)

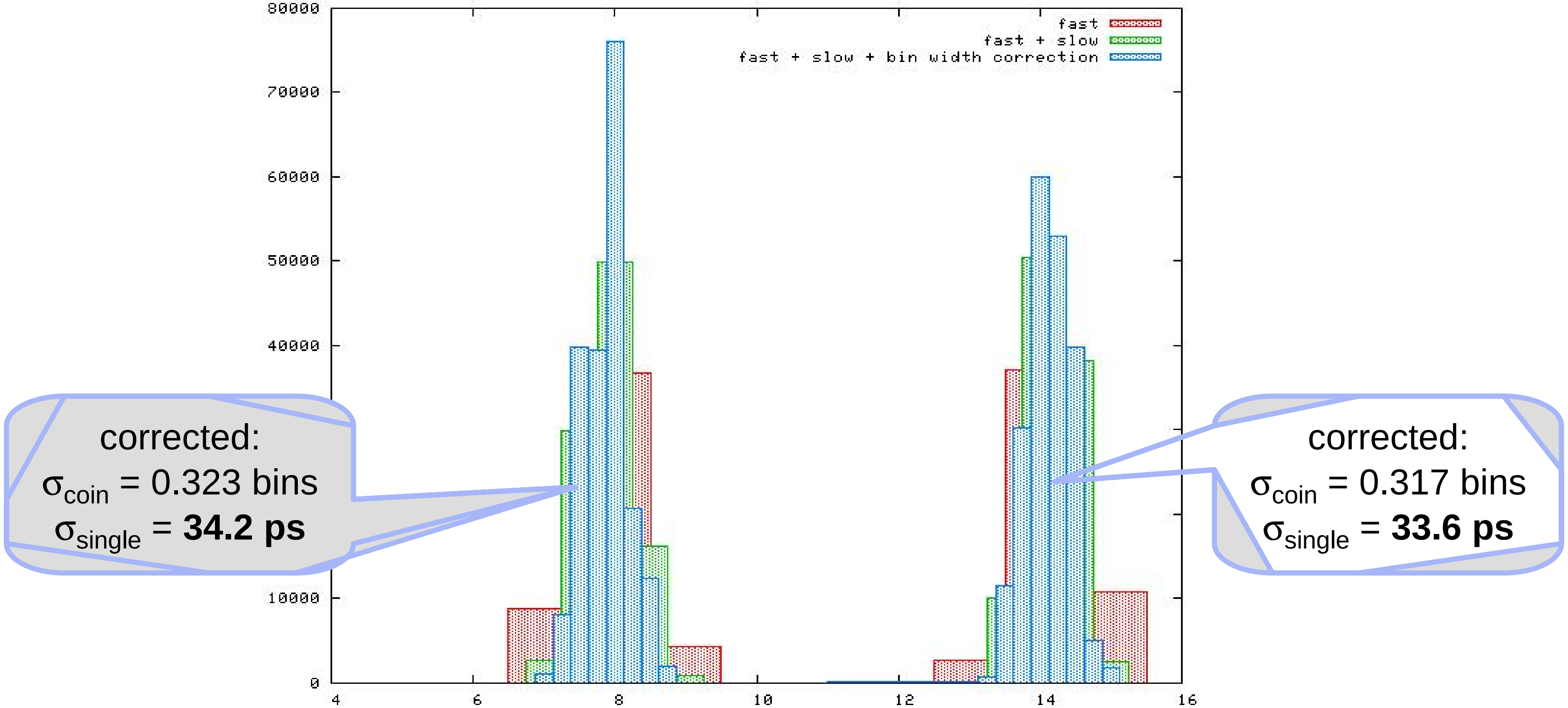
- Generate hits at random moments. Display counts for both channels
  - Equal time bin widths would give homogeneous bin occupancy
  - Shorter bins have lower occupancy



- This measurement used to **correct for bin size**
- variations are from transistor mismatch and stable in time – a chip ‘fingerprint’

Bin width correction

- Use bin width information (fast / slow / mixed) for correction
- result can be further optimized by adjusting delay of the slow buffer…



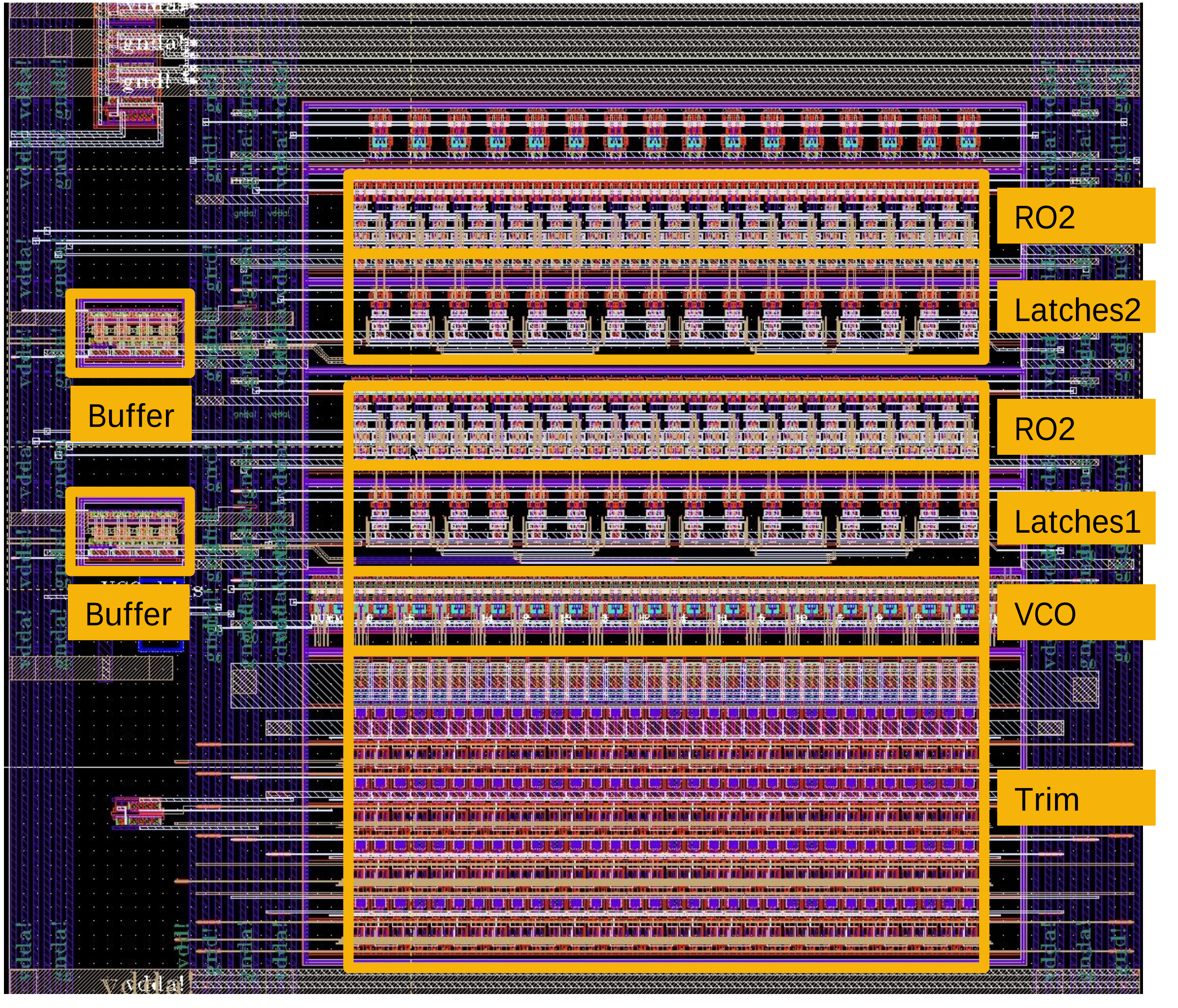
- any non-linearities are included in this measurement!

Next Test Chip: UMC 0.18µm (GSI Submission)

- 16 stages
- 2 groups of latches
- VCO with or without delay trim

- VCO: 260 x 30 µm^2
- Trim: 260 x 120 µm^2

Layout: VCO with Trim



Summary and outlook

- Single channel resolution **σ ~ 35ps** already reached in 0.35μm technology
- Expect factor ~2 improvement in 0.18μm, i.e. **σ ~ 25ps** (test chip has only fast bins).
- Next steps:
  - Test UMC chip (we will get it in 1 week!)
  - Increase speed, linearity, resolution – work is in progress